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5. (Currently Amended) A power MOSFET packaged device comprising:

a power MOSFET ~~according to claim 1~~ comprising:

a semiconductor substrate having one of main surface and the other main surface opposite to each other, the semiconductor substrate having a source electrode and a gate electrode provided on the one main surface and a drain electrode provided on the other main surface;

a source terminal layer disposed on the one main surface and joined to the source electrode;

a gate terminal layer disposed on the one main surface and joined to the gate electrode; and

a drain terminal layer disposed on the other main surface and joined to the drain electrode;

wherein the source terminal layer and the gate terminal layer are respectively disposed on the one main surface with such sizes as to fall within the area of the one main surface, and the drain terminal layer is disposed with such a size as to fall within the area of the other main surface, and

a circuit board, wherein

the power MOSFET is packaged in such a manner that the respective main surfaces of the semiconductor substrate in the power MOSFET are substantially normal to a circuit board.

6. (Original) The power MOSFET packaged device according to claim 5, wherein the source terminal layer, the gate terminal layer, and the drain terminal layer in the power MOSFET are respectively brazed to the circuit board with brazing materials.

7. (Original) The power MOSFET packaged device according to claim 5, wherein an encapsulating resin material is provided so as to cover the semiconductor substrate, the source terminal layer, the gate terminal layer, and the drain terminal layer in the power MOSFET.